CLEAN VERSION OF AMENDED SPECIFICATION PARAGRAPHS

QUANTUM WIRE GATE DEVICE AND METHOD OF MAKING SAME
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A field effect transistor (FET) is a fundamental building block of integrated circuits. Where metal oxide on silicon (MOS) devices are approaching the limits of scaling based upon known fundamental technique, optimization of different components has allowed the FET to continue in the process of miniturization. The decrease in supply voltage, however, has caused acceptable performance in the 0.7X scaling to become increasingly elusive. What is needed is a method of achieving gate dimensions that overcome scaling limits of the prior art.

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In accordance with the present invention, a method of forming a device with uniform and closely spaced quantum wires is provided. Figure 2a is an elevational cross-section view of a structure 200 that includes a substrate 12 with a patterned first oxide 14 disposed thereon. Patterned first oxide 14 is precisely spaced apart to allow crowding of quantum wires into a minimum area. In one embodiment, patterned first oxide 14 has a characteristic width, W, in a range from about 50 nm to about 200 nm, preferably about 100 nm. Patterned first oxide 14 has a characteristic pitch, P, in a range from about 150 nm to about 600 nm, preferably about 300 nm. Thus, where W is equal to a given width X, P is equal to a pitch 3X.